

LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)		ATTY. DOCKET NO.	SERIAL NO.
		100665.0044US2	10/026,337
		APPLICANT	
		Jesse Pedigo	
FILING DATE	GROUP		
12/20/01	1732		

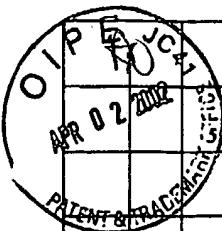
U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AJ	5,906,042	05/25/99	Method and Structure to Interconnect Traces of Two Conductive Layers in a Printed Circuit Board	29	852	10/04/95
	5,925,414	07/20/99	Nozzle and Method for Extruding Conductive Paste into High Aspect Ratio Openings	427	282	07/20/99
	5,994,779	11/30/99	Semiconductor Fabrication Employing a Spacer Metallization Technique	257	773	05/02/97
	6,000,129	12/14/99	Process for Manufacturing a Circuit with Filled Holes	29	852	03/12/98
	6,009,620	01/04/00	Method of Making a Printed Circuit Board Having Filled Holes	29	852	07/15/98
	6,079,100	06/27/00	Method of Making a Printed Circuit Board Having Filled Holes and Fill Member for Use Therewith	29	852	05/12/98
	6,090,474	07/18/00	Flowable Compositions and Use in Filling Vias and Plated Through-Holes	428	209	07/18/00
	6,106,891	08/22/00	Via Fill Compositions for Direct Attach of Devices and Method for Applying Same	427	97	12/18/98
	6,138,350	10/31/00	Process for Manufacturing a Circuit Board with Filled Holes	29	852	02/25/98
	6,153,508	11/28/00	Multi-Layer Circuit Having a Via Matrix Interlayer Connection and Method for Fabricating the Same	438	622	02/19/98
	6,276,055	08/21/01	Method and Apparatus for Forming Plugs in Vias of a Circuit Board Layer	29	852	09/24/98
↓	6,281,448	08/28/01	Printed Circuit Board and Electronic Components	174	260	08/10/99
AJ	6,282,782	09/04/01	Forming Plugs in Vias of Circuit Board Layers and Subassemblies	29	852	09/02/99

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	TRANSLATION	
			YES	NO		
EP 0 194 247 A2			—	—		
EP 0 713 358 A2			—	—		

RECEIVED
APR 03 2002
TC 1700

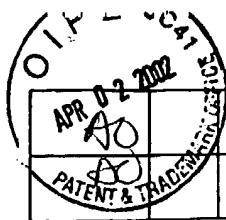


	EP 0723 388 A1 ✓						
	GB 2 120 017 A ✓						
	GB 2 341 347 A ✓						
	GB 2 246 912 A ✓						
	JP 04239193 ✓						
	JP 05275819 ✓						
	JP-53-10487						
	JP 54-139065 ✓						
	JP 62-277794						
	JP 62-287696 ✓						
	JP 03004595 ✓						
	JP 04186792 ✓						
	JP 07176871 ✓						
	JP 08172265 ✓						
	JP 08191184 ✓						
	JP 09321399 ✓						
	JP 09083135 ✓						
	JP 10065339 ✓						
	JP 10256687 ✓						
	JP 11054909 ✓						
	JP 1173696 ✓						
	JP 1236694 ✓						
	JP 58011172 ✓						
	FR 2 684 836						
	FR 2 714 567						
AO	WO 86/06243						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

AJ	Via Etching Process, February 1972
----	------------------------------------

RECEIVED
APR 03 2002
TC 1700



Multilayer Printed Circuit Board Connections, April 1996	
Process for Forming Copper Clad Vias, August 1989	
EXAMINER <i>D. Dwyer</i>	DATE CONSIDERED 4/2004
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

RECEIVED
APR 03 2002
TC 1700

LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>	ATTY. DOCKET NO.	SERIAL NO.
	100665.0044US2	10026,337
	APPLICANT	
	Jesse Pedigo	
	FILING DATE 12/20/01	GROUP 1732

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AD	3,601,523	08/24/71	Through Hole Connectors	174	68.5	06/19/70
	4,106,187	08/15/78	Curved Rigid Printed Circuit Boards	29	625	01/16/76
	4,283,243	08/11/81	Use of Photosensitive Stratum to Create Through-Hole Connections in Circuit Boards	156	237	03/20/80
	4,360,570	11/23/82	Use of Photosensitive Stratum to Create Through-Hole Connections in Circuit Boards	428	596	06/15/81
	4,622,239	11/11/86	Method and Apparatus for Dispensing Viscous Materials	427	96	02/18/86
	4,700,474	10/20/87	Apparatus and Method for Temporarily Sealing Holes in Printed Circuit Boards	29	846	11/26/86
	4,777,721	10/18/88	Apparatus and Method for Temporarily Sealing Holes in Printed Circuit Boards Utilizing a Thermodeformable Material	29	846	10/15/87
	4,783,247	11/8/88	Method and Manufacture for Electrically Insulating Base Material Used in Plated-Through Printed Circuit Panels	204	181.1	05/15/86
	4,884,337	12/05/89	Method for Temporarily Sealing Holes in Printed Circuit Boards Utilizing a Thermodeformable Material	29	846	10/15/87
	4,964,948	10/23/90	Printed Circuit Board Through Hole Technique	156	659	11/13/89
	4,995,941	02/26/91	Method of Manufacture Interconnect Device	156	630	05/15/89
	5,053,921	10/01/91	Multilayer Interconnect Device and Method of Manufacture Thereof	361	386	10/23/90
	5,058,265	10/22/91	Method for Packaging a Board of Electronic Components	29	852	09/10/90
	5,145,691	09/08/92	Apparatus for Packing Filler into Through-Holes or the Like in a Printed Circuit Board	425	110	03/22/91
	5,220,723	06/22/93	Process for Preparing Multi-Layer Printed Wiring Board	29	830	11/04/91
	5,274,916	01/04/94	Method of Manufacturing Ceramic Multilayer Electronic Component	29	848	12/17/92
	5,451,721	09/19/95	Multilayer Printed Circuit Board and Method for Fabricating Same	174	261	09/24/91
AD	5,456,004	10/10/95	Anisotropic Interconnect Methodology for Cost Effective Manufacture of High Density Printed Circuit Boards	29	852	01/04/94
AD	5,471,091	11/28/95	Techniques for Via Formation and Filling	257	752	08/26/91

APR 02 1994

PATENT & TRADEMARK OFFICE

	5,532,516	07/02/96	Techniques for Via Formation and Filling	257	752	03/28/95
	5,540,779	07/30/96	Apparatus for Manufacture of Multi-Layer Ceramic Interconnect Structures	118	692	03/01/95
	5,578,151	11/26/96	Manufacture of A Multi-Layer Interconnect Structure	156	64	03/01/95
	5,591,353	01/07/97	Reduction of Surface Copper Thickness on Surface Mount Printed Wire Boards with Copper Plated Through Holes by the Chemical Planarization Method	216	18	08/18/94
	5,610,103	03/11/97	Ultrasonic Wave Assisted Contact Hole Filling	437	225	12/12/95
	5,637,834	06/10/97	Multilayer Circuit Substrate and Method for Forming Same	174	264	02/03/95
	5,662,987	09/02/97	Multilayer Printed Wiring Board and Method of Making Same	428	209	02/01/96
	5,699,613	12/23/97	Fine Dimension Slacked Vias for a Multiple Layer Circuit Board Structure	29	852	09/25/95
	5,744,285	04/28/98	Composition and Process for Filling Vias	430	318	07/18/96
	5,753,976	05/19/98	Multi-Layer Circuit Having a Via Matrix Interlayer Connection	257	774	06/14/96
	5,761,803	06/09/98	Method of Forming Plugs in Vias of A Circuit Board by Utilizing a Porous Membrane	29	852	06/26/96
	5,766,670,	06/16/98	Via Fill Compositions for Direct Attach of Devices and Methods for Applying Same	427	8	11/17/93
	5,822,856	10/20/98	Manufacturing Circuit Boards Assemblies Having Filled Vias	29	832	06/28/96
	5,824,155	10/20/98	Method and Apparatus for Dispensing Viscous Material	118	410	11/08/95

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES	NO	

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED
	4/2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>		ATTY. DOCKET NO. 100665.0044US2	SERIAL NO. 10/026337
		APPLICANT Jesse Pedigo	
		FILING DATE December 20, 2001	GROUP 1732
		<i>RECEIVED JUN 11 2002</i>	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>KD</i>	4,945,313	07/31/90	Synchronous Demodulator Having Automatically Tuned Band-Pass Filter	329	349	06/05/89
	5,117,069	05/26/92	Circuit Board Fabrication	174	261	09/28/90
	5,133,120	07/28/92	Method of Filling Conductive Material into Through Holes of Printed Wiring Boards	29	852	03/15/91
	5,277,854	01/11/94	Methods and Apparatus for Making Grids from Fibers	264	86	06/06/91
	5,332,439	07/26/94	Screen Printing Apparatus for Filling Through-Holes in Circuit Board With Paste	118	213	08/18/92
	5,707,575	01/13/98	Method for Filling Vias in Ceramic Substrates with Composite Metallic Paste	264	104	07/28/94
	5,744,171	04/28/98	System for Fabricating Conductive Epoxy Grid Array Semiconductor Packages	425	110	05/12/97
	5,753,976	05/19/98	Multi-Layer Circuit Having a Via Matrix Interlayer Connection	257	774	06/14/96
	6,015,520	01/18/00	Method for Filling Holes in Printed Wiring Boards	264	104	05/15/97
	6,149,857	11/21/00	Method of Making Films and Coatings Having Anisotropic Conductive Pathways Therein	264	429	12/22/98
	6,184,133	02/06/01	Method of Forming an Assembly Board With Insulator Filled Through Holes	438	667	02/18/00
<i>KD</i>	6,261,501	07/17/01	Resin Sealing Method for a Semiconductor Device	264	272.15	01/22/99

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YEB	NO	
<i>KD</i>		WO 00/13474					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

--	--	--

EXAMINER	DATE CONSIDERED
<i>D. D.</i>	4/2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>		ATTY. DOCKET NO. 100970.665044US2	SERIAL NO. 10/026337
		APPLICANT Pedigo, Jesse	
		FILING DATE 20 December 2001	GROUP 1732 <i>To be determined</i>

*O P E JC73
APR 25 2003
PATENT & TRADEMARK OFFICE*

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>AC</i>	AA	6,193,144	02/27/01	Paste Providing Methods, Soldering Method and Apparatus and System Therefor	228	248	01/22/98
<i>RD</i>	BB	6,491,204	12/10/02	Stencil Wiping Device	228	22	11/22/00
	CC						
	DD						
	EE						
	FF						
	GG						
	HH						
	II						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO
	JJ						
	KK						
	LL						
	MM						
	NN						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>RD</i>	OO	Shoki Oikawa, et al., Solder Coating Device, December 1, 1988
EXAMINER	<i>Q. Clark</i>	DATE CONSIDERED <i>4/2004</i>

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

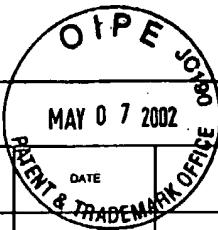
LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>	ATTY. DOCKET NO.	SERIAL NO.
	100665.0044US2	10/026337
	APPLICANT	
	Jesse Pedigo	
	FLING DATE December 10, 2001	GROUP 1732

RECEIVED

MAY 10 2002


U.S. PATENT DOCUMENTS
TC 1700

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AD	5,954,313	09/04/90	Method and Apparatus for Filling High Density Vias	419	9	02/03/89
	5,117,069	05/26/92	Circuit Board Fabrication	174	261	09/28/90
	5,133,120	07/28/92	Method of Filling Conductive Material Into Through Holes of Printed Wiring Boards	29	852	03/15/91
	5,145,691	09/08/92	Apparatus for Packing Filler into Through-Holes or the Like in a Printed Circuit Board	425	110	03/22/91
	5,277,854	01/11/94	Methods and Apparatus for Making Grids from Fibers	264	86	06/06/91
	5,332,439	07/26/94	Screen Printing Apparatus for Filling Through-Holes in Circuit Board with Paste	118	213	08/18/92
	5,540,779	07/30/96	Apparatus for Manufacture of Multi-Layer Ceramic Interconnect Structures	118	692	03/01/95
	5,578,151	11/26/96	Manufacture of a Multi-Layer Interconnect Structure	156	64	03/01/95
	5,610,103	03/11/97	Ultrasonic Wave Assisted Contact Hole Filling	437	225	12/12/95
	5,707,575	01/13/98	Method for Filling Vias in Ceramic Substrates with Composite Metallic Paste	264	104	07/28/94
	5,744,171	04/28/98	System for Fabricating Conductive Epoxy Grid Array Semiconductor Packages	425	110	05/12/97
	5,766,670	06/16/98	Via Fill Compositions for Direct Attach of Devices and Methods for Applying Same	427	8	11/17/93
	5,851,344	12/22/98	Ultrasonic Wave Assisted Contact Hole Filling	156	379.6	09/24/96
	5,925,414	07/20/99	Nozzle and Method for Extruding Conductive Paste into High Aspect Ratio Openings	427	282	02/12/97
	6,015,520	01/18/00	Method for Filling Holes In Printed Wiring Boards	264	104	05/15/97
	6,149,857	11/21/00	Method of Making Films and Coatings Having Anisotropic Conductive Pathways Therein	264	429	12/22/98
	6,184,133	02/06/01	Method of Forming an Assembly Board with Insulator Filled Through Holes	438	667	02/18/00
AD	6,261,501	07/17/01	Resin Sealing Method for a Semiconductor Device	264	272.15	01/22/99



FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES
							NO

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED

4/2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.